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VLSI BASED ACTIVE-GM-RC ANALOG FILTER FOR WIRELESS COMMUNICATION

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ABSTRACT

A VLSI based highly efficient active-Gm-RC analog filter used for various devices like UMTS and WLAN applications has been presented. The fourth order highly efficient analog filter is included in the receiver path of a reconfigurable terminal. The filter is designed by the cascade of two active-Gm-RC biquad blocks. A single op-amp is used for each biquad and its unity-gain-bandwidth is comparable to the filter cut-off frequency. Thus, the filter power consumption is strongly reduced w.r.t. other closed-loop filter configurations. In addition, the filter can be programmed in order to process UMTS and WLAN signals. A Fourth order low pass analog filter with 2 MHz cut-off frequency and a DC gain of 44 dB for UMTS receiver has been designed in 0.18µm CMOS technology with a ±0.8 V supply voltage. The filter has a power dissipation of 98 µW for UMTS and 161 µW for WLAN. The filter has input referred noise (spot noise) of 13.25µV at 2 MHz.

KEYWORDS: Analog Filters, CMOS, Low Voltage, UMTS, WLAN

INTRODUCTION

An Active-Gm-RC analog filter is a three terminal device which is used in telecommunication systems. The baseband filter is a channel selection filter used for low-pass. This low voltage Active-Gm-RC filter in direct conversion receiver select the desired signal following RF mixer without any distortion and rejects the out-of-band signal. So it is also called channel selection filter. A fourth order Active-Gm-RC low pass filter is presented. Active-Gm-RC technique is used because MOSFET-C ones have high linearity performance requirement. So the need of op-amp bandwidth much larger than the filter cut-off frequency leads to high power consumption. As an alternative Gm-C filters reduce the power uses but have lower linearity. The Active-Gm-RC approach for realizing the filter is therefore proposed here in which both linearity is high and power consumption is reduced. The filter consists of op-amps and passive elements. The op-amp frequency response is taken into account in the synthesis of overall transfer function of filter where the op-amp frequency response is fixed and the external components are designed as a function of op-amp frequency response. This makes the overall transfer function to fully depend on the op-amp.

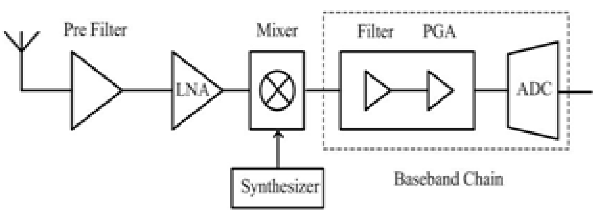

Figure 1: Block Diagram of DCR

LOW PASS FILTER

The active-Gm-RC structure is proposed. The filter consists of two biquad blocks connected in cascade. The figure shows the biquad block using active-Gm-RC technique. It is equivalent to second order low pass filter. The op-amp used in the structure is having a single pole transfer function given by:

$$A(s) = \frac{A_0}{1+sT}$$

Where 1/T and A_0 are the first pole angular frequency and DC gain of op-amp. The op-amp unity gain frequency is given by:

$$\omega = \frac{A_0}{T}.$$

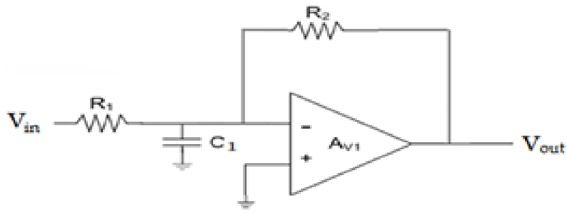

Figure 2: Active-Gm-RC Biquad Block

The Butterworth transfer function is used for large stop band attenuation and in band maximum flat frequency response.

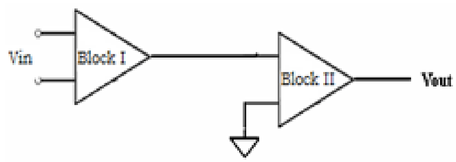

Figure 3: Block Diagram of 4th Order Active-Gm-RC

The transfer function for the filter using Butterworth Approximation is as shown below –$(s^2 + 0.7654s + 1)\ (s^2 + 1.8478s + 1)$

OPERATIONAL AMPLIFIER DESIGN

The Operational Amplifier used in biquad block is a differential input, single ended output Amplifier. It consists of two stages. The first stage is a NMOS Differential-input with PMOS load, single-ended output stage. The second stage is a common source gain stage that has an active load. Capacitor C_c (called miller capacitor) is included to ensure stability when op-amp is used with feedback.

The gain of first stage is given by: $Av_1 = gm1\ (rds2 \| rds4)$

The gain of second stage is given by: $Av_2 = -gm7\ (rds6 \| rds7)$

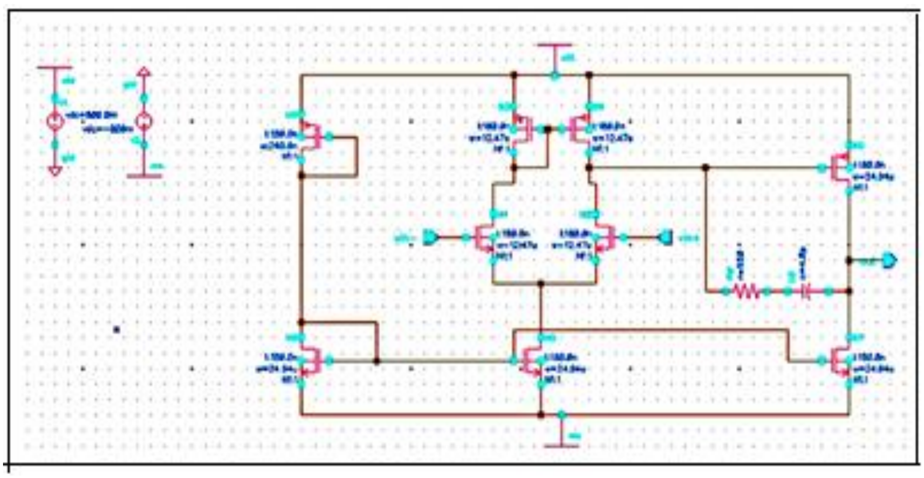

Figure 4: Schematic of op-amp

Filter Design

Figure 5 shows the structure of the fourth-order UMTS/WLAN reconfigurable filter. It is the cascade of two Active-Gm-RC biquad blocks. The challenge of this design is the realization of an efficient dual-mode filter in terms of power and area occupation, operating with a supply voltage limited to ±0.8V, while guaranteeing the large linear range required by the UMTS/WLAN standards. The filter can be reconfigured in order to adjust the filter bandwidth to the selected standard (2 MHz and 8 MHz for UMTS and WLAN standards, respectively).

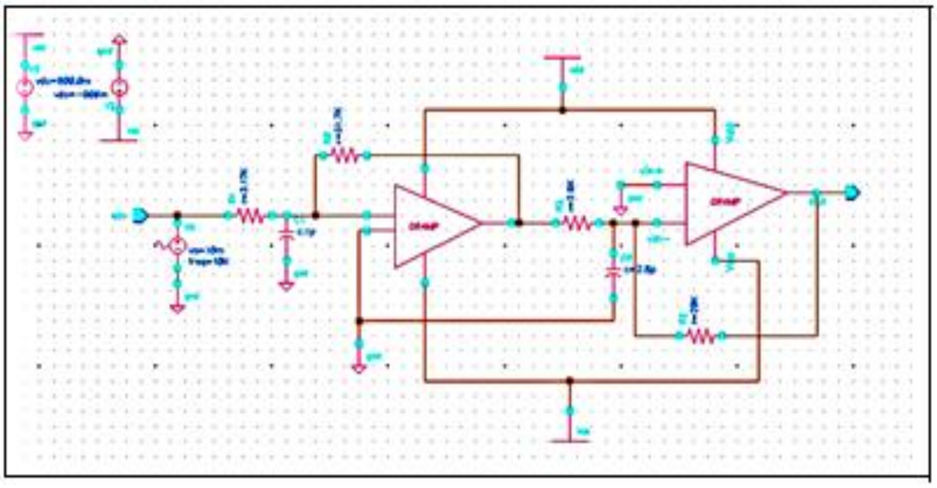

Figure 5: Fourth Order Active-Gm-RC Filte

The Transfer function is given by-

$$T(s) = \frac{G}{\frac{S^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1} \qquad G = \frac{R_2}{R_1}$$

$$Q = \frac{1}{1+G}\sqrt{G_u C_1 R_2}v \qquad \omega_0 = \sqrt{\frac{\omega_u}{C_1 R_2}}$$

Where: G = DC gain of block, Q = Quality factor of block, ω_0 = Cut-off frequency of block, ωu = Unity gain frequency of op-amp.

Simulation Results of Overall Filter

The proposed fourth-order filter has been realized in a 0.18µm standard CMOS technology. Figure 6 shows the schematic of active-Gm-RC filter. Here two biquad blocks are connected in cascade. The filter operates with a single 0.8 V supply voltage with 2 MHz cut-off frequency.

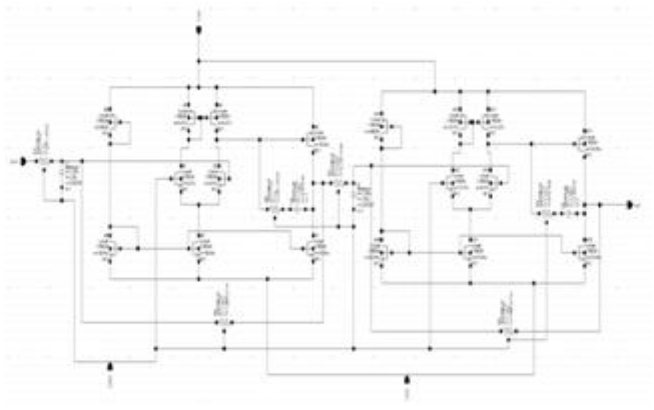

Figure 6: Schematic of Overall Filter

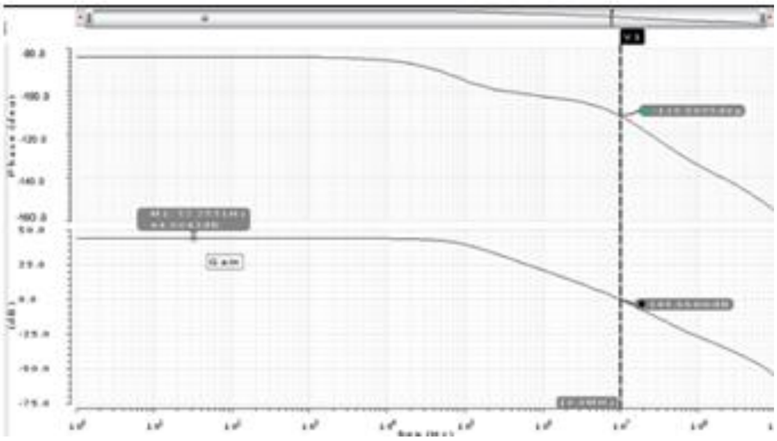

Figure 7: Frequency Response of Overall Filter

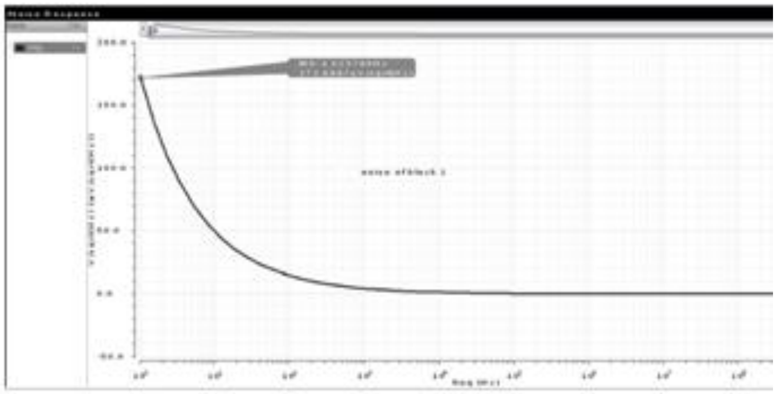

Figure 8: I/P Noise Response of Overall Filter

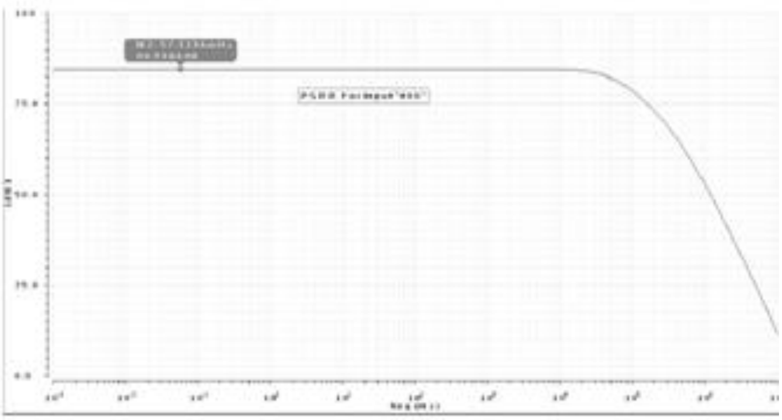

Figure 9: PSRR Response of Overall Filter

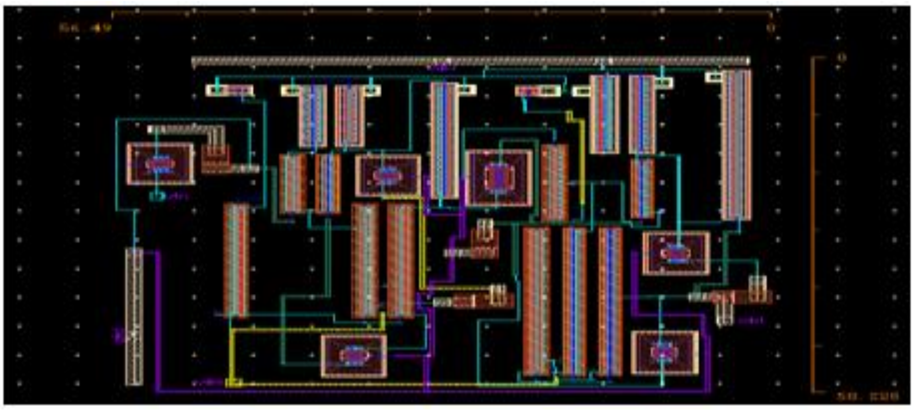

Figure 10: Layout of Overall Filter

CONCLUSIONS

A low voltage fourth order analog baseband filter for telecom receivers has been presented. The filter is able operate at 1.8 V with a 3MHz, -3dB Bandwidth. The filter operates with a good linearity and less noise.

REFERENCES

1. H. Huang and E. K. F. Lee, “Design of low-voltage CMOS continuous time filter with on-chip automatic tuning,” IEEE Journal of Solid-State Circuits, vol. 36, no. 8, pp. 1168-1177, Aug.2001.
2. K. R. Rao, J. Wilson, and M. Ismail, “A CMOS RF front-end for a multistandardWLANreceiver,” *IEEE Microw.Wireless Compon. Lett.*, vol. 15, no. 5, pp. 321–323, May 2005.
3. D. Manstretta, R. Castello, F. Gatta, P. Rossi, and F. Svelto, “A 0.18_m CMOS direct- conversion receiver front-end for UMTS,” in *Proc. IEEE ISSCC*, 2002, pp. 240, 463.
4. S. D’Amico and A. Baschirotto, “Active Gm-RC continuous-time biquadratic blocks,” Analog Integrated Circuits and Signal Processing, vol. 45, no. 3, pp. 1–14, Nov. 2005.
5. S. D’Amico, V. Giannini, and A. Baschirotto, “A 4th-order active Gm-RC reconfigurable (UMTS/WLAN) filter,” *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1630–1637, Jul. 2006.
6. S. Pavan, Y. P. Tsividis, and K. Nagaraj, “Widely programmable high frequency continuous-time filters in digital CMOS technology,” IEEE Journal of Solid-State Circuits, vol. 35,no. 4, pp. 503-511, April 2000.
7. Lo T-Y and Hung C-C, multi mode Gm-C filter channel selections filter for mobile applications in 1V supply voltage, *IEEE trans circuits and systems*-II: *Express Briefs*, 55 (2008) 314-318

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